FIG. **2** is an enlarged cross-sectional view of a diode **30**;

FIG. **3** is a circuit diagram of the semiconductor device **10**;

FIG. **4** is a flow chart of processes that a gate controller circuit **60** executes;

FIG. **5** is a graph showing changes in gate potential Vg according to an embodiment;

FIG. **6** is a graph showing changes in gate potential Vg according to a modification; and

FIG. **7** is a diagram showing an internal circuit of the diode **30**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

FIG. **1** shows a semiconductor device **10** according to an embodiment. The semiconductor device **10** includes a semiconductor substrate **12**. The semiconductor substrate **12** includes an element region **14***a* and an element region **14***b*. In the element region **14***a*, an emitter electrode **16***a* is provided on an upper surface **12***a* of the semiconductor substrate **12**. In the element region **14***b*, an emitter electrode **16***b* is provided on an upper surface **12***a* of the semiconductor substrate **12**. The emitter electrode **16***b*may be linked to or separated from the emitter electrode **16***a*. A collector electrode **18** is provided on a lower surface **12***b* of the semiconductor substrate **12**.

In both the element regions **14***a* and **14***b*, a plurality of trenches is provided in the upper surface **12***a* of the semiconductor substrate **12**. In each of the trenches, a gate insulating film and a gate electrode are provided. In the both element regions **14***a* and **14***b*, n-type emitter regions, a p-type body region, an n-type drift region, a p-type collector region, and the like are provided inside the semiconductor substrate **12**. IGBTs (Insulated Gate Bipolar Transistors) are formed by these regions, the gate insulating films, the gate electrodes, the emitter electrodes **16***a* and **16***b*, and the collector electrode **18** in the element regions **14***a* and **14***b*, respectively.

A portion of the upper surface **12***a* of the semiconductor substrate **12** located between the emitter electrodes **16***a* and **16***b* is covered with an insulating layer **20**. On the insulating layer **20**, gate wires **22** and a diode **30** are provided. The gate wires **22** are configured of n-type polysilicon. The gate wires **22** connect each gate electrode of the IGBTs to a gate pad (not illustrated). The diode **30** is a diode configured to sense a temperature of the semiconductor substrate **12**. The diode **30** is fixed to the upper surface **12***a* of the semiconductor substrate **12** via the insulating layer **20**. The diode **30** will be described in detail later.

On the insulating layer **20**, an insulating layer **24** is provided. The insulating layer **24** covers the gate wires **22** and the diode **30**. For clarification, FIG. **1** shows thicknesses of the diode **30** and the insulating layer **24** in an exaggerated manner.

Provided on top of the semiconductor substrate **12** are a solder layer **48** and a heatsink **50**. The heatsink **50** is a metal plate. The heatsink **50** bridges over the emitter electrode **16***a*, the diode **30**, and the emitter electrode **16***b*. The heatsink **50** is connected to the emitter electrodes **16***a* and **16***b* by the solder layer **48**. That is, the heatsink **50** is connected to the upper surface **12***a* of the semiconductor substrate **12** via the solder layer **48** and the emitter electrodes **16***a*and **16***b*. The heatsink **50** is connected to the semiconductor substrate **12** at positions located on both sides of the diode **30**. This causes the heatsink **50** to be fixed to the semiconductor substrate **12**.

As shown in FIG. **2**, the diode **30** includes a cathode electrode **32**, an n-type semiconductor layer **34**, a p-type semiconductor layer **36**, an anode electrode **38**, and a cathode wiring layer **40**.

The cathode electrode **32** is provided on the insulating layer **20**. The cathode electrode **32** is insulated from the semiconductor substrate **12** by the insulating layer **20**. The cathode electrode **32** is configured of n-type polysilicon. The cathode electrode **32** includes a stacked portion **32***a*and an extension portion **32***b*. The stacked portion **32***a*is a portion on which the n-type semiconductor layer **34**, the p-type semiconductor layer **36**, and the anode electrode **38** are stacked, and the extension portion **32***b*is a portion extending outward from the stacked portion **32***a*along a planar direction of the semiconductor substrate **12**.

The n-type semiconductor layer **34** is provided on the stacked portion **32***a*of the cathode electrode **32**. The n-type semiconductor layer **34** is not provided on the extension portion **32***b*. The n-type semiconductor layer **34** is configured of n-type polysilicon. The n-type semiconductor layer **34** has a density of n-type impurities equal to or lower than a tenth of a density of n-type impurities in the cathode electrode **32** (that is, the cathode electrode **32** has a density of n-type impurities ten or more times higher than a density of n-type impurities in the n-type semiconductor layer **34**). An electric resistivity of the n-type -polysilicon is inversely proportional to a density of n-type impurities in that polysilicon. For this reason, an electric resistivity of the n-type semiconductor layer **34** is ten or more times higher than an electric resistivity of the cathode electrode **32** (that is, the electric resistivity of the cathode electrode **32** is equal to or lower than a tenth of the electric resistivity of the n-type semiconductor layer **34**). Thus, the electric resistivity of the cathode electrode **32** is lower than the electric resistivity of the n-type semiconductor layer **34**.

The p-type semiconductor layer **36** is provided on the n-type semiconductor layer **34**. The p-type semiconductor layer **36** is configured of p-type polysilicon. An electric resistivity of the p-type semiconductor layer **36** is ten or more times higher than the electric resistivity of the cathode electrode **32** (that is, the electric resistivity of the cathode electrode **32** is equal to or lower than a tenth of the electric resistivity of the p-type semiconductor layer **36**). Thus, the electric resistivity of the cathode electrode **32** is lower than the electric resistivity of the p-type semiconductor layer **36**.

The anode electrode **38** is provided on the p-type semiconductor layer **36**. The anode electrode **38** is configured of metal (e.g. AlSi). An electric resistivity of the anode electrode **38** is equal to or lower than a tenth of the electric resistivity of the n-type semiconductor layer **34**, and is equal to or lower than a tenth of the electric resistivity of the p-type semiconductor layer **36**. The anode electrode **38** is connected to an external device at an unillustrated position.

As described above, the diode **30** has a stacked structure in which the stacked portion **32***a*of the cathode electrode **32**, the n-type semiconductor layer **34**, the p-type semiconductor layer **36**, and the anode electrode **38** are stacked along a thickness direction of the semiconductor substrate **12**.

The cathode wiring layer **40** is provided on the extension portion **32***b*of the cathode electrode **32**. The cathode wiring layer **40** is configured of metal (e.g. AlSi). The cathode wiring layer **40** is connected to an external device at an unillustrated position.

FIG. **3** is a circuit diagram of the semiconductor device **10**. The circuit shown in FIG. **3** is a circuit configured to drive an IGBT **62** of the semiconductor substrate **12**. Although a plurality of IGBTs is formed inside the semi-